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ABSTRACT

PROBLEM TO BE SOLVED: To obtain a board for a *high*-*density* area *grid* *array* package whereon a semiconductor chip with many pins can be mounted by simple means.

SOLUTION: An area *grid* *array* package-oriented board having a first layer 1 with pads 7, a second layer 2 connected with the first layer 1 and for mounting a semiconductor chip 10 thereon, and an *insulation* layer 3 interposed between the first and second layers 1, 2, wherein after the first layer 1 is removed by a laser beam machining to the rear surface of the second layer 2 through the interposed *insulation* layer 3 to form via-holes 6 with tapered sections in the layers 1, 3, *platings* 5 for the *via* -holes 6 are applied thereto from their opening surfaces, and then, while etching both the sides of the board, the pads 7 are formed in the form of grid points in the first layer 1 and wirings 8 and lands 9 which are connected with both the chip 10 and via-holes 6 are formed in the second layer 2. Hereupon, it is possible that each via-*hole* 6 has *no* *filling* for each pad 7 to have a recessed portion or each via-*hole* 6 has a *filling* to make each pad 7 plane-form.

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(71) Applicant: **FUJI KIKO DENSHI KK**

(72) Inventor: **HIRAKAWA TADASHI**

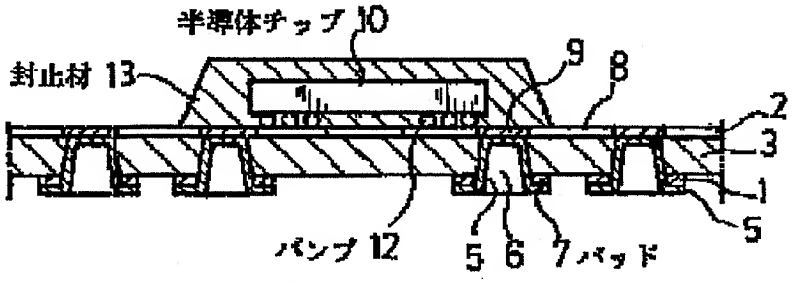
(74) Representative:

(54) BOARD FOR AREA GRID ARRAY PACKAGE AND ITS MANUFACTURE

(57) Abstract:

PROBLEM TO BE SOLVED: To obtain a board for a high-density area grid array package whereon a semiconductor chip with many pins can be mounted by simple means.

SOLUTION: An area grid array package-oriented board having a first layer 1 with pads 7, a second layer 2 connected with the first layer 1 and for mounting a semiconductor chip 10 thereon, and an insulation layer 3 interposed between the first and second layers 1, 2, wherein after the first layer 1 is removed by a laser beam machining to the rear surface of the second layer 2 through the interposed insulation layer 3 to form via-holes 6 with tapered sections in the



with tapered sections in the layers 1, 3, platings 5 for the via-holes 6 are applied thereto from their opening surfaces, and then, while etching both the sides of the board, the pads 7 are formed in the form of grid points in the first layer 1 and wirings 8 and lands 9 which are connected with both the chip 10 and via-holes 6 are formed in the second layer 2. Hereupon, it is possible that each via-hole 6 has no filling for each pad 7 to have a recessed portion or each via-hole 6 has a filling to make each pad 7 plane-form.